AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A display driver apparatus for driving a display comprising a plurality of pixels, each of which is located at a respective one of a plurality of intersections formed ~~between one~~by an arrangement of a plurality of common electrodes positioned generally parallel to one another and extending in a first direction and one of a plurality of segment electrodes positioned generally parallel to one another and extending in a second direction, wherein an orientation state of an electro-optical material of each pixel is controlled by a voltage applied to it, the display driver apparatus comprising:

a common electrode drive device that supplies a scanning signal for simultaneously selecting L common electrodes, where L is a natural number and $L \geqq 2$;

a segment electrode drive device that supplies a data signal to each of the plurality of segment electrodes;

a storage medium from which N-bit display data are simultaneously read out for ~~each~~ the L pixels at the respective L intersections that each of the plurality of segment electrodes form with the L common electrodes that are simultaneously selected, the storage medium including a memory address space in which the display data is organized according to the groups of L commonly selected electrodes and bit positions for pixels in the selected groups; and

a decoder having a plurality of sub-decoders and that divides the N-bit display data simultaneously read out from the storage medium into (N/L)-bit data units, decodes the (N/L)-bit data units, and outputs a voltage to be applied to each of the segment electrodes;

wherein

in a first mode, the N-bit display data provides 2^A display gradients for each of L pixels on each of the segment electrodes, where $A = (N/L) \geqq 2$, and an output voltage is output from a selected one of the sub-decoders in each of A divided periods of one horizontal scanning period, and

in a second mode, the N-bit display data provides 2^B display gradients for each of n × L pixels on each of the segment electrodes, where $1 \leqq B = A/n$ and $n \geqq 2$, and an output voltage is output from a selected one of the sub-decoders every n horizontal scanning periods.

2. (Currently Amended) A display driver apparatus according to claim 1, further comprising a terminal that selects ~~one of~~ the first mode ~~and~~ or the second mode.

3. (Currently Amended) A display driver apparatus according to claim 1, further comprising an interface circuit for inputting the N-bit display data from an external source, wherein a mode selection signal for selecting ~~one of~~ the first mode ~~and~~ or the second mode is input through the interface circuit.

4. (Original) A display driver apparatus according to claim 1, wherein in the first mode the N-bit display data provides four display gradients for each of L pixels on each of the segment electrodes.

5. (Original) A display driver apparatus according to claim 4, wherein in the second mode the N-bit display data provides two display gradients for each of 2L pixels on each of the segment electrodes.

6. (Original) An electro-optical device comprising a display driver apparatus according to claim 1.

7. (Original) An electronic device comprising an electro-optical device according to claim 6.

8. (Currently Amended) A method for driving a display comprising a plurality of pixels, each of which is located at a respective one of a plurality of intersections formed between one of a plurality of common electrodes and one of a plurality of segment electrodes, wherein an orientation state of an electro-optical material of each pixel is controlled by a voltage applied to it, the display driving method comprising the steps of:

a common electrode drive device that supplies a scanning signal for simultaneously selecting L common electrodes, where L is a natural number and $L \geqq 2$;

supplying a data signal to each of the plurality of segment electrodes;

simultaneously reading from a memory N-bit display data for each of the plurality of segment electrodes, the memory having an address space in which the display data is organized according to the groups of commonly selected electrodes and bit positions for pixels in the selected groups; and

dividing each read N-bit display data into (N/L)-bit units, decoding the (N/L)-bit data units, and output a voltage to be applied to each of the segment electrodes;

wherein

in a first mode, the N-bit display data provides 2^A display gradients for each of L pixels on each of the segment electrodes, where $A = (N/L) \geqq 2$, and an output voltage is output in each of A divided periods of one horizontal scanning period, and

in a second mode, the N-bit display data provides 2^B display gradients for each of $n \times L$ pixels on each of the segment electrodes, where $1 \leqq B = A/n$ and $n \geqq 2$, and an output voltage is output every n horizontal scanning periods.

9. (Currently Amended) A display driving method according to claim 8, further comprising the steps of inputting the N-bit display data from an external source, and inputting a mode selection signal for selecting ~~one of~~ the first mode ~~and~~ or the second mode from an external source.

10. (Original) A display driving method according to claim 8, wherein in the first mode the N-bit display data provides four display gradients for each of L pixels on each of the segment electrodes.

11. (Original) A display driving method according to claim 10, wherein in the second mode the N-bit display data provides two display gradients for each of 2L pixels on each of the segment electrodes.

REMARKS

This Response is submitted together with a request for continued examination (RCE). Claims 1-11 are pending. The preamble of each of independent claims 1 and 8 has been amended to more clearly define the arrangement of common electrodes and segment electrodes, as well as the intersections where the pixels are located. A clarifying amendment has also been made to each of these claims regarding the N-bit display data. Each of claims 2, 3 and 9 has been amended to employ the disjunctive "or" where appropriate. No change in scope to any of the claims is intended by any of these amendments.

Claims 1-11 remain rejected under 35 U.S.C. § 103(a) based on JP 11-149278 (*Shingo*), which is directed to a liquid crystal driver that is capable of changing between a 4 gradation display and a binary display. Paragraphs [0034] – [0038] in the machine translation of *Shingo* discuss the decoder, 4 gradation display operation and binary display operation.

However, there is an important difference between the present invention and the liquid crystal driver of *Shingo*. That difference lies in the arrangement of display data in a memory address space. The difference is illustrated using the tables below.

Table 1(a): portion of Fig. 6(B) in *Shingo*

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
[0]	a1L	a1H	b1L	b1H	c1L	c1H	d1L	d1H	a2L	a2H	b2L	b2H	c2L	c2H	d2L	d2H
[1]	e1L	e1H	f1L	f1H	g1L	g1H	h1L	h1H	e2L	e2H	f2L	f2H	g2L	g2H	h2L	h2H

In *Shingo* the suffix "L" denotes a lower bit and the suffix "H" denotes an upper bit. Since the present invention uses a different notation system, i.e., "-1" denotes an upper bit and "-2" denotes a lower bit, Table 1(a) is rewritten to employ the notation of this invention for comparison purposes. The result is Table 1(b) below.

Table 1(b): Table 1(a) rewritten using the notation of the present invention

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
[0]	a1-2	a1-1	b1-2	b1-1	c1-2	c1-1	d1-2	d1-1	a2-2	a2-1	b2-2	b2-1	c2-2	c2-1	d2-2	d2-1
[1]	e1-2	e1-1	f1-2	f1-1	g1-2	g1-1	h1-2	h1-1	e2-2	e2-1	f2-2	f2-1	g2-2	g2-1	h2-2	h2-1

Table 2: portion of Fig. 5 in the present application

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
[0]	a1-1	b1-1	c1-1	d1-1	a1-2	b1-2	c1-2	d1-2	a2-1	b2-1	c2-1	d2-1	a2-2	b2-2	c2-2	d2-2
[1]	e1-1	f1-1	g1-1	h1-1	e1-2	f1-2	g1-2	h1-2	e2-1	f2-1	g2-1	h2-1	e2-2	f2-2	g2-2	h2-2

Comparing Table 1(b), which represents arrangement of *Shingo's* memory address space, with Table 2, which represents a memory address according to the present invention, it is easy to see that they are quite different. Unlike the memory address space in *Shingo*, the memory address space in applicants' invention is arranged such that the display data is organized according to the groups of L commonly selected electrodes and bit positions for pixels in the selected groups. For example, in the illustrated arrangement, line [0] contains L (=4 here) upper bits of display data, one for each of the L pixels corresponding to the intersection of a first segment electrode and the L common electrodes selected in a first selection period, followed by the L corresponding lower bits for those pixels. The next eight bits in line [0] are for the L pixels corresponding to the intersection of a second segment electrode and that same group of L common electrodes selected in the first selection period. Each of independent claims 1 and 8 has been amended to further emphasize this difference between the present invention and *Shingo*.

Arranging the data as set forth in claim 1, together with employing the other claimed features, a single display driver apparatus having improved general applicability is achieved. The memory space in the display driver apparatus is arranged to allow a greater variety of display data to be stored, such that the apparatus can be controlled, for example, to more smoothly perform a scroll display on the liquid crystal panel.

As further recited in the claims, the two claimed modes of operation provide different display gradients, each precisely defined by device-related variables. The first mode provides $2^A = 2^{(N/L)}$ display gradients for each of the L pixels on each of the segment electrodes, where N is the number of bits in the display data, L is the number of common electrode simultaneously selected by the scanning signal, and N/L denotes the number of bits in each data unit. The second mode provides $2^B = 2^{(N/L)(1/n)}$ display gradients for each of n × L pixels on each of the segment electrodes. In the first mode, a selected one of the sub-decoders outputs a voltage in each of A divided periods in one horizontal scanning period. In the second mode, a selected one of the sub-decoders outputs a voltage every n horizontal scanning periods. This arrangement wherein multiple display modes are interrelated and the frequency of the voltage output in a given mode is related to its corresponding display gradient as shown above advantageously provides the claimed display driver with more versatility and general applicability than that of prior display drivers including the one shown in *Shingo*.

Accordingly, it is respectfully submitted that each of the independent claims 1 and 8 is patentably distinguishable over *Shingo*, and that each of the remaining dependent claims is patentable for at least the same reasons as its independent claim. In view of the foregoing, applicants respectfully request favorable reconsideration of the present application.

Respectfully submitted,

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